BRIEF DATASHEET

PART NUMBER: CT4948A21962D1

DESCRIPTION: NAND FLASH 2Gb (x8)+
DDR3(L) SDRAM 4Gb (x32)

CHIPSIP Technology Co., Ltd.

ChipSiP Technology Co., Ltd.
8F-1, No. 186, Jian 1st Rd, Zhonghe District, New Taipei City 235, Taiwan
Tel: 886-2-8227-1799 Fax: 886-2-8227-1798
E-mail: sales@ChipSiP.com
www.ChipSiP.com

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Using This Document

This document is intended for hardware and software engineer’s general information on the CT4948A21962D1 .Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Revision History

Revision	Date	Description
Rev 0.1	2016/06/14	Create new document
Rev 0.2	2016/09/05	Modified 1.2 Features:NAND FLASH Block size

1. INTRODUCTION

CT4948A21962D1 is a Multi Chip Package Memory (MCP) that integrated 2G bits NAND Flash and 2G bits DDR3(L) SDRAM x2 by advanced SiP (System-in-a-Package) technology. CT4948A21962D1 offers space saving advantage that could miniaturize your portable device, and it is conformed with Green regulations.

1.1 Application

- Compact DSC / CAR Black Box / Action Cam / 360 Cam
- Drone
- Wearable

1.2 Features

PRODUCT LIST

- CT4948A21962D1
  - ■ NAND FLASH: 2G bits (256M x 8-bit)
  - ■ DDR3(L) SDRAM: 4G bits (16M x 8-Bank x32-bit)

POWER SUPPLY

- NAND FLASH
  - ■2.7-3.6V
- DDR3(L) SDRAM
  - ■DDR3L: 1.35V (1.283–1.45V) / Backward-compatible to DDR3: 1.5V ±0.075V

PACKAGE

- ●FBGA 10.5 x 13.5 x 1.4mm, 148 Balls
- ●Ball Pitch: 0.8 mm
- ●Weight: 332mg +/-5mg

Temperature

- Operating: -10 to +85 °C
- Storage: -55 to +125°C

NAND FLASH

- Density
  - ■2Gbit
- ●Architectur
- Single-level Cell(SLC) Technology
- OPEN NAND FLASH INTERFACE(ONFI)1.0 COMPLIANT
- POWER SUPPLY VOLTAGE
  - ■VCC = 2.7V ~ 3.6V
- MEMORY CELL ARRAY (with SPARE)
  - ■ Page size
    - X8 : (2K+128spare) bytes
  - ■Block size
    - X8 : (128K+8K) bytes
  - ■ Plane size : 1024blocks
  - ■ Device size : 2048blocks
- PAGE READ / PROGRAM
  - ■ Random Read Time(tR) : 30us(Max)
  - ■ Sequential access time
    - 3.3V Device:25ns(Min)
  - ■ Page program
    - 3.3V Device : 300us(Typ)
  - ■ Multi-page program(2 pages)
    - 3.3V Device : 300us(Typ)
- BLOCK ERASE
  - ■ Block erase time: 3.5ms(Typ)
  - ■ Multi-block erase(2 Blocks)
    - 3.3V Device : 3.5ms(Typ)
- COMMAND SET
  - ■ ONFI1.0 Compliant command set
  - ■ Read Unique ID
- SECURITY
  - ■ OTP area
  - ■ Serial number(unique ID)
  - ■ Non-volatile protection
- ELECTRONIC SIGNATURE
  - ■ 1st cycle: Manufacturer Code
  - ■ 2nd cycle: Device Code

- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
- 4th cycle: Page size, Block size, Organization, Spare size, Serial Access Time
- 5th cycle: ECC, Multi-plane information

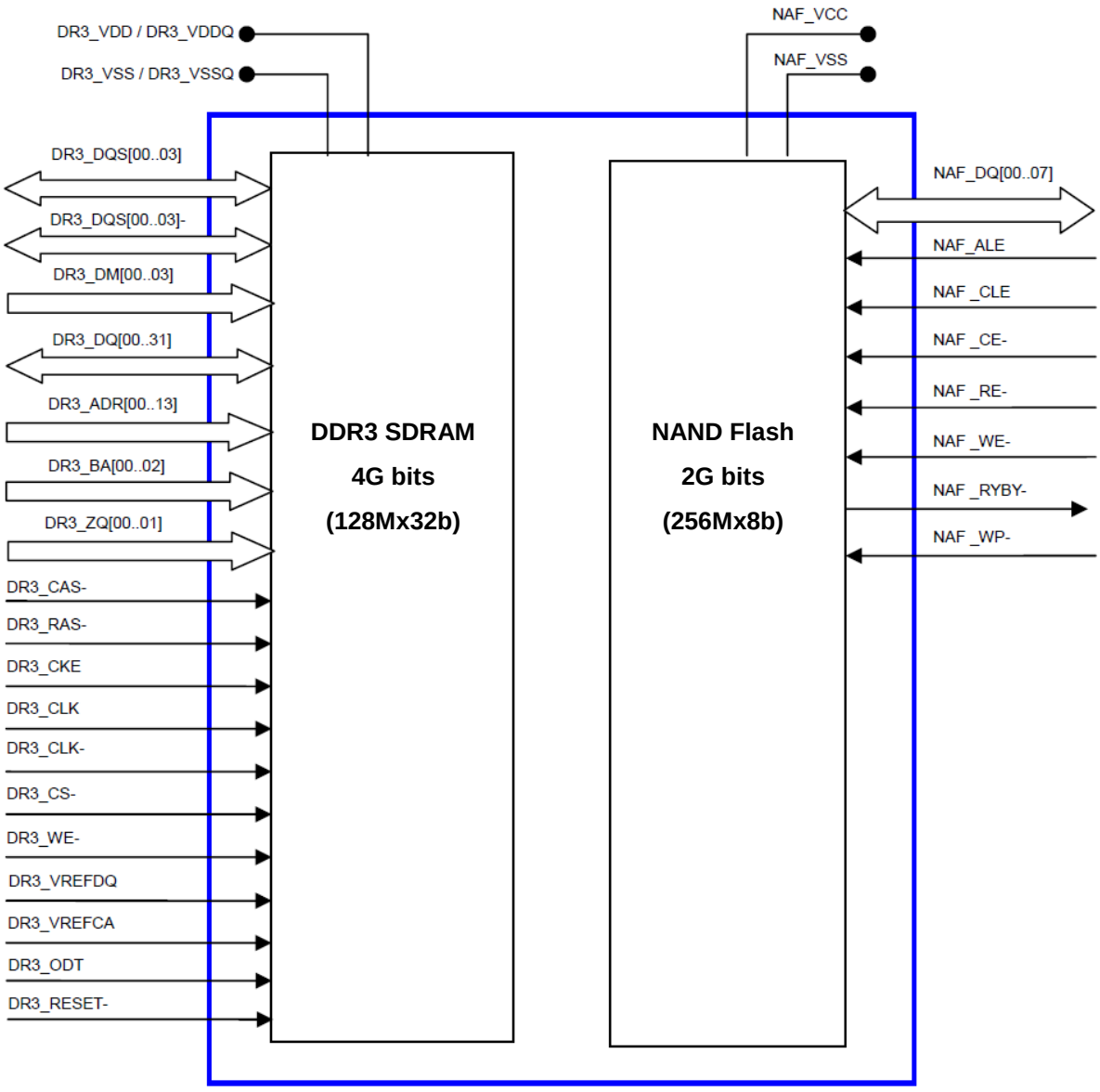
- RELIABILITY
  - 50,000 Program / Erase cycles (with 4bit/512 ECC)
- DATA RETENTION
  - 10 years

DDR3(L) SDRAM

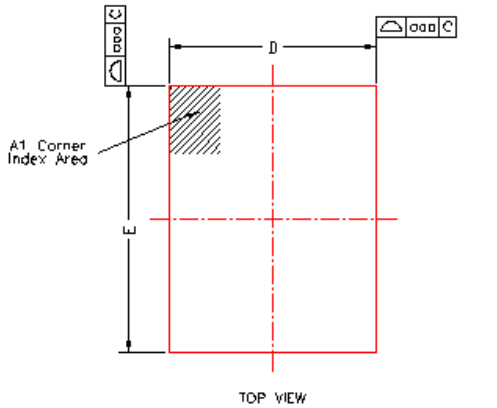
- DDR3L: V_{DD} = V_{DDQ} = 1.35V (1.283–1.45V)
- Backward-compatible to DDR3: V_{DD} = V_{DDQ} = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on $_{t}$CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of -10°C to 95°C
  - 64ms, 8192 cycle refresh at -10°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration
- Page size
  - 2KB
- DDR3L: only for 1.35V parameters, setting, or description
- DDR3: only for 1.5V parameters, setting, or description
- DDR3(L): both of them can use the same parameters, setting, or description

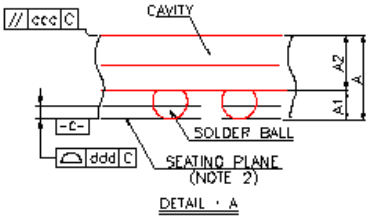
2. FUNCTION DIAGRAM

2.1 MCP

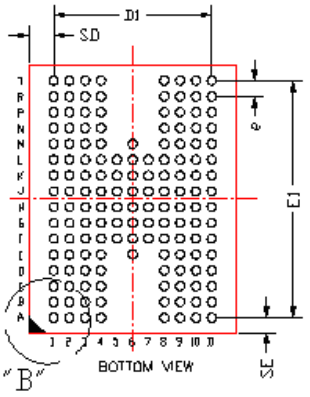


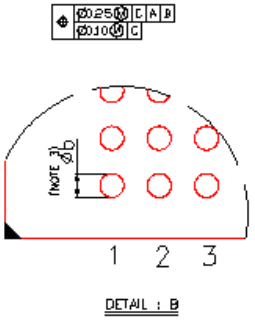
3. PACKAGE DIMENSION (148 Ball FBGA, 10.5x13.5x1.4mm)





Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---		1.40
A1	0.32	0.37	0.42
A2	---	---	0.98
D	10.40	10.50	10.60
E	13.40	13.50	13.60
D1	---	8.00	---
E1	---	12.00	---
SD	---	1.25	---
SE	---	0.75	---
e	---	0.80	---
b	0.40	0.45	0.50
n	148		
aaa		0.15	
ccc		0.20	
ddd		0.12	





NOTE :
1. CONTROLLING DIMENSION : mm.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

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